ELEC2301: Unit Outline

Unit Coordinator

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Other pages about this Unit:


Supplementary assessment is not available in this unit except in the case of a bachelor’s pass degree student who has obtained a mark of 45 to 49 and is currently enrolled in this unit, and it is the only remaining unit that the student must pass in order to complete their course.

Outcomes

Students are able to design and understand digital systems; illustrate problem formulation and solution; work as an individual or as a member of a team; and develop self-learning skills, communication and report writing skills.

This unit builds on the introductory material in ELEC1300 Digital Systems 1 (formerly 620.102 Computer Engineering 102/ENGT1300 Computer Engineering) to teach the principles of good logic design and to develop the knowledge and skills necessary for the design of robust digital electronic systems. In particular, students develop a sound understanding of the principles of good logic design and become proficient in the use of VHDL as a design tool; are able to design robust digital systems using modern computer-aided engineering (CAE) tools; use a systems approach to design; understand timing issues; appreciate issues of product testing and techniques used to improve testability; and use programmable logic devices such as CPLD.

Content

This unit covers the use of VHDL to describe, design and validate digital systems; sequential circuits and finite state machines; races and hazards in sequential circuits; timing considerations; product testing, fault diagnosis and design for testability; and programmable logic devices.

Pre-requisites and Co-requisites (unit specific, technical and software)

CITS1210 C Programming or CITS1220 Software Engineering (formerly 670.104 Software Engineering 104) or CITS1200 Java Programming (formerly 230.120 Java Programming 124) and ELEC1300 Digital Systems 1 (formerly 620.102 Computer Engineering 102/ENGT1300 Computer Engineering)

Unit Structure and assessment

Assessment:

<table>
<thead>
<tr>
<th>Type</th>
<th>% of final mark</th>
<th>Week due in each Semester</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test #1</td>
<td>20%</td>
<td>Week 7</td>
</tr>
<tr>
<td>Test #2</td>
<td>20%</td>
<td>Week 12</td>
</tr>
<tr>
<td>Lab assignments</td>
<td>15%</td>
<td>ongoing</td>
</tr>
<tr>
<td>Final Exam</td>
<td>45%</td>
<td></td>
</tr>
</tbody>
</table>

These dates are subject to change